

ABSTRACT

A signal router routes N inputs to M outputs. All inputs signals are ultimately applied to a data buss by spreading across multiple buss lines and time multiplexing. The data are read from the buss and written in identical images to K random access memories. The memories are addressed and read according to a different schedule for each of K output signals that are ultimately demultiplexed to M outputs. As each RAM image is read, another RAM image is written and vice versa. Since each RAM image contains the same data, the generation of signals from each RAM to supply each of the respective K output signals can be done at a rate that is substantially more independent of the input, buss, or RAM write operations than prior art techniques permit.

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